

METAL OXIDE SEMICONDUCTOR (MOS) BANDGAP VOLTAGE REFERENCE CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to bandgap voltage generators, and in particular, to bandgap voltage generators using metal oxide semiconductor (MOS) devices.

2. Description of the Related Art

[0002] Bandgap voltage generator circuits are well known in the art and can be implemented using many circuit topologies. As is well known, the circuit relies on two transistors (generally implemented as two groups of mutually interconnected transistors) running at different emitter current densities, with the current-rich transistor typically running at ten or more times the density of the current-lean transistor. Such a factor of ten or more will cause a 60-millivolt difference between the base-emitter voltages V_{be} of the two transistors/groups. This difference voltage is then typically amplified by a corresponding factor of ten or more and added to another base-emitter voltage. The total of these two voltages add up to approximately 1.22 volts, which is approximately the bandgap of silicon.

[0003] Present bandgap voltage generators now typically use MOS devices as part of a larger MOS circuit. However, as is well known, many implementations of MOS devices result in the creation of parasitic bipolar junction transistors which can produce undesirable parasitic effects, such as circuit latchup or parasitic capacitance which affects circuit startup and operation.

SUMMARY OF THE INVENTION

[0004] In accordance with the presently claimed invention, a metal oxide semiconductor (MOS) bandgap voltage reference circuit includes a plurality of dummy bipolar junction transistors (BJTs) coupled to the mismatched parasitic substrate BJTs for improving parasitic capacitance matching, thereby improving startup behavior of the bandgap reference circuitry.

[0005] In accordance with one embodiment of the presently claimed invention, a metal oxide semiconductor (MOS) bandgap voltage reference circuit includes MOS bandgap voltage generator circuitry and a plurality of dummy transistors. The MOS bandgap voltage generator circuitry includes: first and second parasitic substrate transistor circuits with first and second base terminals, first and second emitter terminals, first and second collector terminals, and first and second emitter areas, respectively; and a first resistance coupled between the first and second base terminals. The first emitter area is greater than the second emitter area and one of the first emitter and collector terminals is mutually coupled with a like one of the second emitter and collector terminals. The plurality of dummy transistors includes mutually coupled base terminals coupled to the second base terminal, and mutually coupled emitter terminals and mutually coupled collector terminals coupled to the mutually coupled first and second parasitic substrate transistor circuit terminals.

[0006] In accordance with another embodiment of the presently claimed invention, a MOS bandgap voltage reference circuit includes MOS current source circuitry, parasitic substrate transistor circuitry, a resistance, amplifier circuitry, resistive circuitry and a plurality of dummy transistors. The MOS current source circuitry includes a control terminal and first, second, third and fourth output terminals, and is responsive to a control signal by providing

an output voltage via the first output terminal, substantially equal first and second source currents via the second and third output terminals, and first and second source voltages via the third and fourth output terminals. First parasitic substrate transistor circuitry is coupled to the second output terminal and includes first base, emitter and collector terminals and a first emitter area. Second parasitic substrate transistor circuitry is coupled to the third output terminal and includes second base, emitter and collector terminals and a second emitter area, wherein the first emitter area is greater than the second emitter area, and one of the second emitter and collector terminals is mutually coupled with a like one of the first emitter and collector terminals. The resistance is coupled between the first and second base terminals. The amplifier circuitry is coupled to the third and fourth output terminals and the control terminal, and is responsive to the first and second source voltages by providing the control signal. The resistive circuitry is coupled to the first output terminal, the second base terminal and the mutually coupled first and second parasitic substrate transistor circuitry terminals. The plurality of dummy transistors includes mutually coupled base terminals coupled to the second base terminal, and mutually coupled emitter terminals and mutually coupled collector terminals coupled to the mutually coupled first and second parasitic substrate transistor circuitry terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 is a schematic diagram of a MOS bandgap voltage reference circuit with compensation for parasitic capacitances of the substrate bipolar junction transistors (BJTs) used for generating the bandgap voltage in accordance with one embodiment of the presently claimed invention.

[0008] Figures 1A and 1B illustrate cross-sectional views of an integrated circuit containing MOS transistors in which parasitic substrate BJTs are formed.

[0009] Figure 2 is a schematic diagram illustrating in more detail the introduction of dummy transistors for providing compensation in accordance with one embodiment of the presently claimed invention.

[0010] Figure 3 is a plan view of a portion of an integrated circuit containing the substrate and dummy BJTs for providing compensation in accordance with one embodiment of the presently claimed invention.

[0011] Figure 4 is a signal timing diagram illustrating differences in performance of the circuit of Figure 1 with and without the use of dummy transistors.

DETAILED DESCRIPTION

[0012] The following detailed description is of example embodiments of the presently claimed invention with references to the accompanying drawings. Such description is intended to be illustrative and not limiting with respect to the scope of the present invention. Such embodiments are described in sufficient detail to enable one of ordinary skill in the art to practice the subject invention, and it will be understood that other embodiments may be practiced with some variations without departing from the spirit or scope of the subject invention.

[0013] Throughout the present disclosure, absent a clear indication to the contrary from the context, it will be understood that individual circuit elements as described may be singular or plural in number. For example, the terms “circuit” and “circuitry” may include either a single component or a plurality of components, which are either active and/or passive and are

connected or otherwise coupled together (e.g., as one or more integrated circuit chips) to provide the described function. Additionally, the term “signal” may refer to one or more currents, one or more voltages, or a data signal. Within the drawings, like or related elements will have like or related alpha, numeric or alphanumeric designators.

[0014] Referring to Figure 1, one example of a bandgap voltage generator circuit which can be compensated in accordance with the presently claimed invention is a common form of circuit often referred to as a “Brokaw bandgap circuit.” Such a circuit is implemented using complementary MOS devices with mismatched parasitic substrate PNP BJTs Q1, Q2. A differential amplifier A1 controls the gate terminal of a P-type MOS transistor M1 which serves as a controllable current source. This causes a channel current to flow in transistor M1 such that node voltages V+, V- at the lower terminals of resistors RA1 and RA2 are equal. Resistors RA1 and RA2 are equal, thereby causing the currents I through transistors Q1 and Q2 to be equal. In the event that the node voltages V+, V- begin to differ, the differential amplifier action of the error amplifier A1 will cause the source current 2I to be modified such that these voltages V+, V- remain equal.

[0015] As a result, the voltage across resistor Rdelta at the emitter terminal of transistor Q1 can be as expressed below in Equation 1:

$$\text{Eq. 1: } V_{\text{rdelta}} = V_{\text{eb2}} - V_{\text{eb1}} - I_{\text{base}} \cdot R_{\text{base}}$$

[0016] The currents I in transistors Q1 and Q2 are equal, therefore the difference in their respective emitter-base voltages Vbe1, Vbe2 can be expressed as follows (where VT is the thermal voltage, and A1 and A2 are the respective emitter areas of transistors Q1 and Q2):

$$\text{Eq. 2: } V_{\text{eb2}} - V_{\text{eb1}} = V_T \cdot \ln(A1/A2)$$

[0017] A base current Ibase is expressed below in Equation 3:

$$\text{Eq. 3: } I_{\text{base}}(Q1) = I / \beta(Q1)$$

[0018] Thus, the voltage across resistor R_{delta} is as expressed below in Equation 4 (where emitter areas 44 and 5 for this example have been substituted for $A1$ and $A2$, respectively):

$$\text{Eq. 4: } V_{\text{rdelta}} = V_T \ln(44/5) - I * R_{\text{base}} / \beta(Q1)$$

[0019] A voltage across resistor R_{delta} is also equal to:

$$\text{Eq. 5: } V_{\text{rdelta}} = I * R_{\text{delta}}$$

[0020] Setting Equations 4 and 5 equal to each other allows the current parameter I to be isolated and expressed as:

$$\text{Eq. 7: } I = V_T \ln(44/5) / (R_{\text{delta}} + R_{\text{base}} / \beta(Q1))$$

[0021] Assuming that the resistances and the β of transistor $Q1$ do not vary greatly with temperature, the current I is a PTAT (proportional to absolute temperature) current. Solving for the voltage difference between the output voltage V_{out} and node voltage V_M :

$$\text{Eq. 8: } V_{\text{bg}} = V_{\text{out}} - V_M = V_{\text{eb2}} + I * (R_{A2} + 2 * R_B)$$

[0022] The emitter-base voltage V_{eb2} of transistor $Q2$ will decrease approximately 2 millivolts per degree Celsius, so a value of $(R_{A2} + 2R_B)$ can be selected such that the voltage difference between the output voltage V_{out} and node voltage V_M will not vary linearly with temperature. This voltage difference V_{bg} between the output voltage V_{out} and node voltage V_M in such case is approximately equal to the bandgap voltage of silicon (1.22 volts).

[0023] The current through resistor $R2$ in the resistive output circuit is equal to:

$$\text{Eq. 9: } I(R2) = V_{\text{bg}} / R1 + 2 * I_{\text{base}}$$

[0024] By multiplying this current $I(R2)$ by the resistance $R2$ and adding the resulting voltage to the bandgap voltage V_{bg} , the output voltage V_{out} can be computed:

$$\text{Eq. 10: } V_{out} = V_{bg}(1 + R2/R1) + 2 \cdot I_{base} \cdot R2$$

[0025] Solving for the bandgap voltage V_{bg} in terms of the remaining circuit voltages and substituting this into Equation 10 yields:

$$\begin{aligned} \text{Eq. 11: } V_{out} = & (1 + R2/R1) \cdot [(V_{be2} + V_T \cdot \ln(44/5) \cdot (R_{A2} + 2R_B)/R_{\Delta}) \\ & + I_{base} \cdot (2 \cdot R1/R2 - R_{base} \cdot (R_{A2} + 2R_B)/R_{\Delta})] \end{aligned}$$

[0026] This equation shows that the term I_{base} for the current through the base resistance R_{base} can be eliminated by proper selection of the value for the base resistance R_{base} (this base resistance R_{base} is used for base current compensation for transistors $Q1$ and $Q2$):

$$\text{Eq. 12: } R_{base} = 2 \cdot R1/R2 \cdot R_{\Delta} / (R_{A2} + 2R_B)$$

[0027] Equation 10 then reduces to:

$$\text{Eq. 13: } V_{out} = V_{bg} \cdot (1 + R2/R1)$$

[0028] This circuit has two stable operating points: one in which the output voltage V_{out} is as expressed in Equation 13, and the other in which the output voltage is zero volts. To avoid the operating state of $V_{out} = 0$ volts, this circuit must be started up or forced to reach the desired operating condition (as per Equation 13). A common technique for doing this is using a startup circuit to pull down the gate terminal of the source current transistor $M1$ so as to force transistor $M1$ to begin conducting and supplying current to the circuit. After a predetermined time interval has elapsed or a predetermined output voltage V_{out} has been achieved, the startup circuit returns control to the amplifier $A1$.

[0029] Included as part of this bandgap voltage generator circuit, as discussed in more detail below, is a group of “dummy” transistors D for providing compensation for parasitic capacitances associated with the substrate transistors Q1, Q2.

[0030] Referring to Figures 1A and 1B, parasitic substrate transistors, such as those transistors Q1, Q2 used in the circuit of Figure 1 for generating the bandgap voltage, are often formed as a result of the fabrication of MOS transistors. As is shown, in this case using a typical complementary MOS transistor inverter circuit as an example, an N-well is implanted or diffused within a P-substrate, followed by implantation or diffusion of additional P+ and N+ regions for creating the P-type and N-type MOS transistors in accordance with well known semiconductor fabrication techniques. The P-substrate forms the collector of a vertical PNP transistor T1. The N-well acts as the base of the PNP transistor T1. The P+ sources and drains of the P-channel MOS transistor serve as the emitter of the PNP transistor T1. The N-well is normally connected to the power supply voltage VDD, the most positive circuit voltage, via an N+ diffusion tab, while the substrate is terminated at circuit ground GND, the most negative circuit voltage, through a P+ diffusion. In the present case, the N-well is not connected to the highest potential, but is instead used as the base terminal of the vertical PNP transistor T1. (With the substrate typically at circuit ground potential, no functional lateral NPN transistor will be produced.)

[0031] Referring to Figure 2, the substrate transistors Q1, Q2 have at least two types of parasitic capacitances associated with them. The capacitance C_{dep} between the base and collector terminals is a depletion capacitance which is proportional to the number of transistors in the composite transistor. Accordingly, transistor Q2, which is composed of a smaller number of devices (and thereby serves as the “current-rich device”), has a smaller

depletion capacitance C_{dep} than transistor Q1. The capacitance C_{diff} between the emitter and base terminals is a diffusion capacitance. When the circuit is starting up and the emitter voltages are low, the depletion capacitance C_{dep} dominates over the diffusion capacitance C_{diff} . The diffusion capacitance C_{diff} does not start affecting circuit operation until the emitter-base junction is sufficiently forward biased after startup.

[0032] Upon circuit startup, the base terminal of transistor Q2 will rise in voltage before the base terminal of transistor Q1 due to the difference in depletion capacitances C_{dep} , thereby causing unequal emitter currents to flow through transistors Q1 and Q2. This current imbalance causes a relatively large differential voltage at the input of the error amplifier A1 (Figure 1), which can saturate the amplifier A1, thereby causing the output voltage V_{out} to overshoot the desired value and approach the value of the positive power supply voltage VDD.

[0033] A solution to this current imbalance caused by the parasitic depletion capacitances C_{dep} is to balance the respective depletion capacitances C_{dep} associated with the two transistors Q1, Q2 during initial startup conditions. This can be done by connecting inactive, i.e., dummy, transistors outside the array of transistors forming transistors Q1 and Q2. These dummy transistors will help with matching of the depletion capacitance C_{dep} between transistors Q1 and Q2, as well as add capacitance to output node VM (Figure 1). Each dummy transistor would preferably have a similar depletion capacitance C_{dep} so as to help balance the two transistors Q1, Q2 such that one transistor base will not rise in voltage before the other. (The emitter-base capacitance of the dummy transistors is also a depletion capacitance C_{dep} since the emitter-base junction is reverse biased.)

[0034] Referring to Figure 3, such a modification can be accomplished by providing the dummy transistor D in a substantially symmetrical array surrounding the periphery of the substantially symmetrical array formed by the transistors which collectively form the substrate transistors Q1, Q2, and does not require additional capacitors to be placed within the circuit. An additional benefit is that depletion capacitance added by the dummies will track the depletion capacitance C_{dep} of transistor Q2 and will not adversely affect the circuit after startup.

[0035] Referring to Figure 4, the beneficial effect of avoiding overshoot of the output voltage V_{out} can be seen by comparing the transient responses of the output voltage V_{out} with and without the use of such dummy transistors.

[0036] Various other modifications and alternations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and the spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.